CLAIMS

1. A method for programming a memory cell comprising a first electrode, a second electrode and an inter-electrode layer of material, comprising:

applying stress to the inter-electrode layer to induce a progressive change in a property of said inter-electrode layer.

2. The method of claim 1, wherein said inter-electrode layer comprises a dielectric, and said property is resistance.

3. The method of claim 1, wherein said inter-electrode layer comprises an ultra-thin layer.

4. The method of claim 1, wherein said inter-electrode layer of material comprises silicon dioxide having a thickness less than 20 Angstroms.

5. The method of claim 1, wherein said inter-electrode layer of material comprises silicon oxynitride having a thickness less than 20 Angstroms.

6. The method of claim 1, wherein said inter-electrode layer of material comprises silicon dioxide having a thickness less than 15 Angstroms.

7. The method of claim 1, wherein said inter-electrode layer of material comprises silicon oxynitride having a thickness less than 15 Angstroms.

8. The method of claim 1, wherein said material in said inter-electrode layer of material comprises at least one of Al_2O_3, YTa_2O_5, HfO_2, Y_2O_3, CeO_2, TiO_2, $HfSi_xO_y$, HfSiON, $HfAlO_x$, TaO_xN_y, ZrO_2, $ZrSi_xO_y$, La_2O_3, and ZrO_2.

9. The method of claim 1, including, after applying said stress to cause said progressive change in the property, generating a signal indicating the property, and comparing the signal with a reference signal to verify programming of desired data.

10. The method of claim 1, including, after applying said stress to cause said progressive change in the property, generating a signal indicating the property, and comparing the signal with a reference signal to verify programming of desired data; and

if said verifying fails, then applying stress again to cause additional change in said property.

11. The method of claim 1, wherein said memory cell comprises an element of a memory array, and a plurality of levels of said property are associated with respective numbers of program cycles applied to the memory array, and including:

maintaining a record of a number of program cycles applied to the memory array;

producing a reference signal corresponding with said number of program cycles;

after applying said stress to cause said progressive change in the property, generating a signal indicating the property, and comparing the signal with said reference signal to verify programming of desired data.

12. The method of claim 1, wherein said memory cell comprises an element of a memory array, and a plurality of levels of said property are associated with respective numbers of program cycles applied to the memory array, and including:

maintaining a record of a number of program cycles applied to the memory array;

providing a source of two reference signals corresponding with first and second program cycles;

after applying said stress to cause said progressive change in the property, generating a signal indicating the property, and comparing the signal with a reference signal corresponding with said number of program cycles selected from said two reference signals to verify programming of desired data.

13. The method of claim 1, wherein said memory cell comprises an element of a memory array, and a plurality of levels of said property are associated with respective numbers of program cycles applied to the memory array, and including:

maintaining a record of a number of program cycles applied to the memory array;

providing a source of three reference signals corresponding with first, second, and third program cycles;

after applying said stress to cause said progressive change in the property, generating a signal indicating the property, and comparing the signal with a reference signal corresponding with said number of program cycles selected from said three reference signals to verify programming of desired data.

14. The method of claim 1, wherein said memory cell comprises an element of a memory array, and a plurality of levels of said property are associated with respective numbers of program cycles applied to the memory array, and including:

maintaining a record of a number of program cycles applied to the memory array;

providing a source of a plurality of reference currents corresponding with respective numbers of program cycles;

after applying said stress to cause said progressive change in the property, generating a signal current indicating the property, and comparing the signal current with a selected reference current selected from said plurality of reference currents and corresponding with said number of program cycles, to verify programming of desired data.

15. The method of claim 1, wherein a plurality of levels of said property are associated with respective values of multiple bits of data in the memory cell, and including:

providing a value for said multiple bits of data to be programmed in the memory cell;

producing a reference signal corresponding with said value;

after applying said stress to cause said progressive change in the property, generating a signal indicating the property, and comparing the signal with said reference signal to verify programming of said value.

16. The method of claim 1, wherein a plurality of levels of said property are associated with respective values of multiple bits of data in the memory cell, and including:

providing a value for said multiple bits of data to be programmed in the memory cell;

providing a source of a plurality of reference currents corresponding with respective values for said multiple bits;

after applying said stress to cause said progressive change in the property, generating a signal current indicating the property, and comparing the signal current with a selected reference current selected from said plurality of reference currents and corresponding with said value, to verify programming of said value.

17. The method of claim 1, wherein a plurality of levels of said property are associated with respective values of multiple bits of data in the memory cell, and including:

providing a value for said multiple bits of data to be programmed in the memory cell;

providing a source of three reference currents corresponding with respective values for two bits;

after applying said stress to cause said progressive change in the property, generating a signal current indicating the property, and comparing the signal current with a selected reference current selected from said three reference currents and corresponding with said value, to verify programming of said value.

18. The method of claim 1, wherein a plurality of levels of said property are associated with respective values of multiple bits of data in the memory cell, and including:

providing a value for said multiple bits of data to be programmed in the memory cell;

providing a source of seven reference currents corresponding with respective values for three bits;

after applying said stress to cause said progressive change in the property, generating a signal current indicating the property, and comparing the signal current with a selected reference current selected from said seven reference currents and corresponding with said value, to verify programming of said value.

19. The method of claim 1, wherein after applying said stress, sensing whether said property exceeds a first reference level to indicate a first stored value, and then applying stress another time to cause additional progressive change in said property to change the stored value, and sensing whether said property exceeds a second reference level to indicate the changed stored value.

20. The method of claim 1, wherein said applying stress includes:

applying a first program pulse to the cell having a first pulse height and a first pulse width;

determining whether the cell is programmed in response to the first program pulse; and if not

applying a program retry pulse to the cell;

determining whether the cell is programmed in response to the program retry pulse; and if not

iteratively applying another program retry pulse to the cell and determining whether the cell is programmed, until the cell is determined to be programmed or a maximum number of retries is made;

wherein the program retry pulses have respective pulse widths and pulse heights which vary according to a pattern in which at least one program retry pulse has a different pulse width or different pulse height than other program retry pulses in the pattern.

21. A method for programming a memory array multiple times, comprising:

applying stress to selected memory cells in said array to set values of a property of said selected memory cells;

maintaining a record of a number of program cycles applied to said array;

producing a reference signal corresponding with said number of program cycles, wherein said reference signal is changed progressively for succeeding program cycles;

after applying said stress, generating a signal indicating the value of said property programmed in a selected memory cell, and comparing the signal with said reference signal to sense data stored in the selected memory cell.

22. The method of claim 21, wherein said providing a reference signal includes:

providing a source of two reference signals corresponding with first and second program cycles, and selecting one of the two reference signals for the first program cycle and selecting the other of the two reference signals for the second program cycle.

23. The method of claim 21, wherein said providing a reference signal includes:

providing a source of first and second sets of reference signals, said first and second sets corresponding with respective first and second program cycles, and said first and second sets comprising respective pluralities of reference signals corresponding with respective values for multiple bits of data stored in the selected memory cell;

selecting a reference signal from the first set for the first program cycle and selecting a reference signal from the second set for the second program cycle.

24. The method of claim 21, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer has a property characterized by a progressive change in said property in response to said stress.

25. The method of claim 21, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second

electrode and an inter-electrode layer, and said inter-electrode layer comprises an ultra-thin layer.

26. The method of claim 21, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon dioxide less than 20 Angstroms thick.

27. The method of claim 21, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon dioxide less than 15 Angstroms thick.

28. The method of claim 21, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon oxynitride less than 20 Angstroms thick.

29. The method of claim 21, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon oxynitride less than 15 Angstroms thick.

30. A method for resetting data stored in a memory array, where data in the memory array is stored by setting a property of memory cells in the array above or below a reference level to indicate a data value, comprising:

changing the reference level.

31. The method of claim 30, wherein said changing the reference level resets data stored in the array without changing said property in memory cells in the array.

32. The method of claim 30, wherein said changing the reference level comprises changing a reference used for sensing a level of said property of memory cells in the array.

33. The method of claim 30, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said property comprises resistance, and wherein said changing the reference level comprises changing a reference current used for sensing a level of resistance of memory cells in the array.

34. The method of claim 30, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer is characterized by a progressive change in said property in response to said stress.

35. The method of claim 30, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises an ultra-thin layer.

36. The method of claim 30, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon dioxide less than 20 Angstroms thick.

37. The method of claim 30, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon dioxide less than 15 Angstroms thick.

38. The method of claim 30, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon oxynitride less than 20 Angstroms thick.

39. The method of claim 30, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon oxynitride less than 15 Angstroms thick.

40. A method for programming data stored in a memory array multiple times, comprising:

setting a property of memory cells in the array above or below a first reference level to indicate data values in said memory cells;

resetting the array by changing the reference level to a second reference level; and

setting the property of memory cells in the array above or below the second reference level to indicate said data values in said memory cells.

41. The method of claim 40, wherein said changing the reference level comprises changing a reference used for sensing a level of said property of memory cells in the array.

42. The method of claim 40, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer is characterized by a progressive change in said property in response to said stress.

43. The method of claim 40, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said property comprises resistance, and

wherein said changing the reference level comprises changing a reference current used for sensing a level of resistance of memory cells in the array.

44. The method of claim 40, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises an ultra-thin layer.

45. The method of claim 40, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon dioxide less than 20 Angstroms thick.

46. The method of claim 40, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon dioxide less than 15 Angstroms thick.

47. The method of claim 40, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon oxynitride less than 20 Angstroms thick.

48. The method of claim 40, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon oxynitride less than 15 Angstroms thick.

49. A method for programming multiple bits of data in memory cells in a memory array multiple times, comprising:

setting a property of memory cells in the array above or below a first set of reference levels to indicate multiple bits of data in said memory cells;

resetting the array by changing the first set of reference levels to a second set of reference levels; and

setting the property of memory cells in the array above or below the second set of reference levels to indicate said multiple bits of data in said memory cells.

50. The method of claim 49, wherein said changing the first set of reference levels to the second set of reference levels comprises changing references used for sensing levels of said property of memory cells in the array.

51. The method of claim 49, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said property comprises resistance, and wherein said changing the first set of reference levels to the second set of reference levels comprises changing reference currents used for sensing levels of resistance of memory cells in the array.

52. The method of claim 49, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer is characterized by a progressive change in said property in response to said stress.

53. The method of claim 49, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises an ultra-thin layer.

54. The method of claim 49, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second

electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon dioxide less than 20 Angstroms thick.

55. The method of claim 49, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon dioxide less than 15 Angstroms thick.

56. The method of claim 49, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon oxynitride less than 20 Angstroms thick.

57. The method of claim 49, wherein said memory array comprises an array of memory cells, and said memory cells respectively comprise a first electrode, a second electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of silicon oxynitride less than 15 Angstroms thick.